CLAIMS

1. A signal flow driven circuit analysis technique by tracing circuit signal flow so that, analyzing a circuit, and partitioning a circuit based on functionality and criticality, and generating multitude circuit layout constraints are done by software program automatically.

2. The signal flow driven circuit analysis technique of claim 1 comprising:
   (a) Providing a memory that is able to store a series of rules in said memory; and
   (b) Storing said series of rules in said memory; and
   (c) Providing a memory that is able to store a circuit netlist employing input/output pin, any other terminal pins, power/ ground terminals, active device elements, and passive device elements; and
   (d) Storing said circuit netlist in said memories; and
   (e) Utilizing said series of rules to trace signal flow information and perform automatic circuit analysis of said circuit netlist; and
   (f) Storing said signal flow information in said memory.

3. The signal flow driven circuit analysis technique of claim 2 further including a partition technique comprising:
   (a) Utilizing the signal flow driven circuit analysis technique of claim 2 wherein said signal flow information to partition the circuit netlist of claim 2 into two parts: digital part and analog/RF part; and
   (b) Providing a memory that is able to store a series of critical signal flow requirements; and
   (c) Storing said series of critical signal flow requirements in said memory; and
   (d) Utilizing said series of critical signal flow requirements to partition said analog/RF part in two parts: a biasing circuit part and a core signal flow path; and
   (e) Utilizing said series of critical signal flow requirements to identify an unit circuit of current mirror, an unit circuit of differential pairs, an unit circuit of

voltage reference, unite circuit of current reference, and an unite circuit of amplifier [etc.]; and

(f) Utilizing said series of critical signal flow requirements to identify multitude critical nodes, multitude critical nets, and multitude critical components in the circuit netlist of claim 2; and

(g) Providing a memory that is able to store said critical nodes, said critical nets, and said critical components; and

(h) Storing said critical nodes, said critical nets, and said critical components in said memory.

4. The signal flow driven circuit analysis technique of claim 1 further including a physical layout constraint generation technique comprising:

(a) Proving a memory that is able to store a series of physical requirement rules; and

(b) Storing said series of physical requirement rules in said memory; and

(c) Utilizing the signal flow driven circuit analysis technique of claim 2 wherein said signal flow information, and the signal flow driven circuit partition technique of claim 3 wherein said critical nodes, said critical nets, said critical components, and said physical requirement rules to generate multitude circuit physical layout constraints of matching, abutment, symmetry, and parasitic loading; and

Whereby an engineer can layout an analog circuit, a mixed signal circuit, and a RF circuit automatically.

5. A mean of circuit performance assessment utilizing:

(a) The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and

(b) The signal flow driven circuit partition technique of claim 3 wherein said critical nodes, and said critical nets, said critical components; and

(c) The physical layout constraint generation technique of claim 4 wherein said physical requirement rules.

6. A mean of circuit yield enhancement utilizing:
   (a) The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and
   (b) The signal flow driven circuit partition technique of claim 3 wherein said critical nodes, and said critical nets, and said critical components; and
   (c) The physical layout constraint generation technique of claim 4 wherein said physical requirement rules to increase yield of analog circuit, and of mixed signal circuit, and of RF circuit.

7. A circuit hierarchy regeneration technique comprising:
   (a) The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and
   (b) The signal flow driven circuit partition technique of claim 3 wherein said digital part, and said analog/RF part, and biasing circuit part, and said core signal flow path, and said unit circuit; and
   (c) The physical layout constraint generation technique of claim 4 wherein said circuit physical layout constraints of matching, abutment, symmetry, and parasitic loading; and

Whereby an engineer can improve an analog circuit, mixed signal circuit, and RF circuit simulation speed.

8. A circuit performance optimization technique utilizing
   (a) The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and
   (b) The signal flow driven circuit partition technique of claim 3 wherein said digital part, and said analog/RF part, and biasing circuit part, and said core signal flow path, and said unit circuit; and
   (c) The physical layout constraint generation technique of claim 4 wherein said circuit physical layout constraints of matching, abutment, symmetry, and

parasitic loading to optimize performance of an analog circuit, and of a mixed signal circuit, and of a RF circuit.

9. A circuit physical layout optimization technique utilizing
   (a) The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and
   (b) The signal flow driven circuit partition technique of claim 3 wherein said digital part, and said analog/RF part, and biasing circuit part, and said core signal flow path, and said unit circuit; and
   (c) The physical layout constraint generation technique of claim 4 wherein said circuit physical layout constraints of matching, abutment, symmetry, and parasitic loading to optimize a layout of analog circuit, and of mixed signal circuit, and RF circuit.

10. A mean of circuit physical layout floor planning utilizing:
   (a) The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and
   (b) The signal flow driven circuit partition technique of claim 3 wherein said digital part, and said analog/RF part, and biasing circuit part, and said core signal flow path, and said unit circuit; and
   (c) The physical layout constraint generation technique of claim 4 wherein said circuit physical layout constraints of matching, abutment, symmetry, and parasitic loading to optimize a layout of analog circuit, and of mixed signal circuit, and RF circuit.

11. A mean of extracting Intellectual Property circuit cell utilizing:
   (a) The signal flow driven circuit analysis technique of claim 2 wherein said signal flow information; and
   (b) The signal flow driven circuit partition technique of claim 3 wherein said digital part, and said analog/RF part, and biasing circuit part, and said core signal flow path, said unit circuit; and

(c) The physical layout constraint generation technique of claim 4 wherein said circuit physical layout constraints of matching, abutment, symmetry, and parasitic loading to reuse an Intellectual Property circuit cell.